SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

A NEW GENERATION OF VERY LOW DROP VOLTAGE REGULATORS

by Riccardo Erckert

Monolithic voltage regulators have become a standard device of modern electronics. Most of today's PC-board designers tend to use them just like transistors or resistors. In reality these versatile devices have a quite complex internal structure. So some basic rules should be respected for their application.

1. A LITTLE BIT OF HISTORY

The first available regulators still had external power transistors. At that time this was the most economic solution to satisfy both technical and economical requirements of the customer. Quite soon the power transistor was integrated. It was implemented as a NPN transistor (mostly in darlington configuration) because integrated NPN transistors can handle significantly higher current densities than lateral PNP transistors. The drawback of this configuration was the required voltage drop between input and output of the regulator in the range of 2V leading to higher power dissipation according to the minimum required drop. The next step was the low drop regulator using an darlington output transistor consisting of a PNP driver and a NPN power transistor. This structure reduced the voltage drop required downto about 1.1V. Then the very low drop regulators using PNP transistors as power transistors became more and more popular. The reason were requirements driven by application such as proper function even at very low input voltages (For example in automotive applications while the starter is working).

2. CHARACTERISTICS OF A STANDARD REGULATOR TOPOLOGY

Fig. 1 shows the block diagram of a standard voltage regulator in application.

Figure 1: Standard Voltage Regulator using a Darlington Output

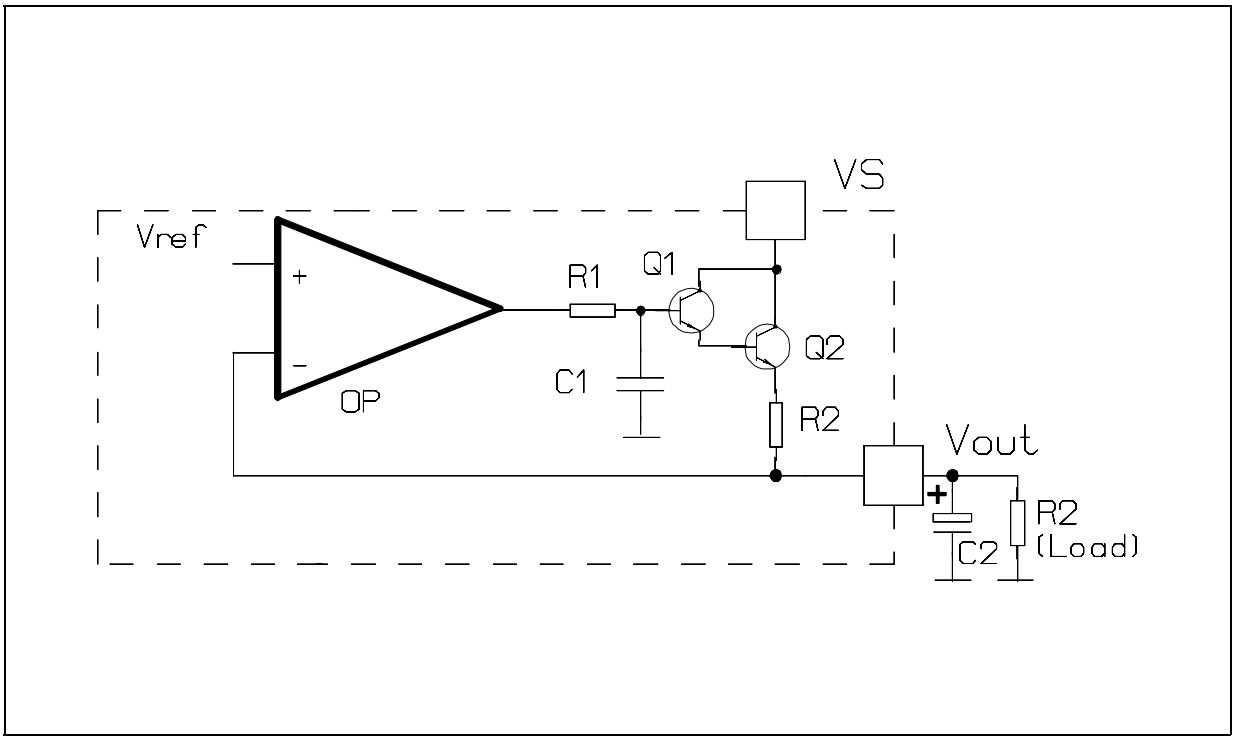
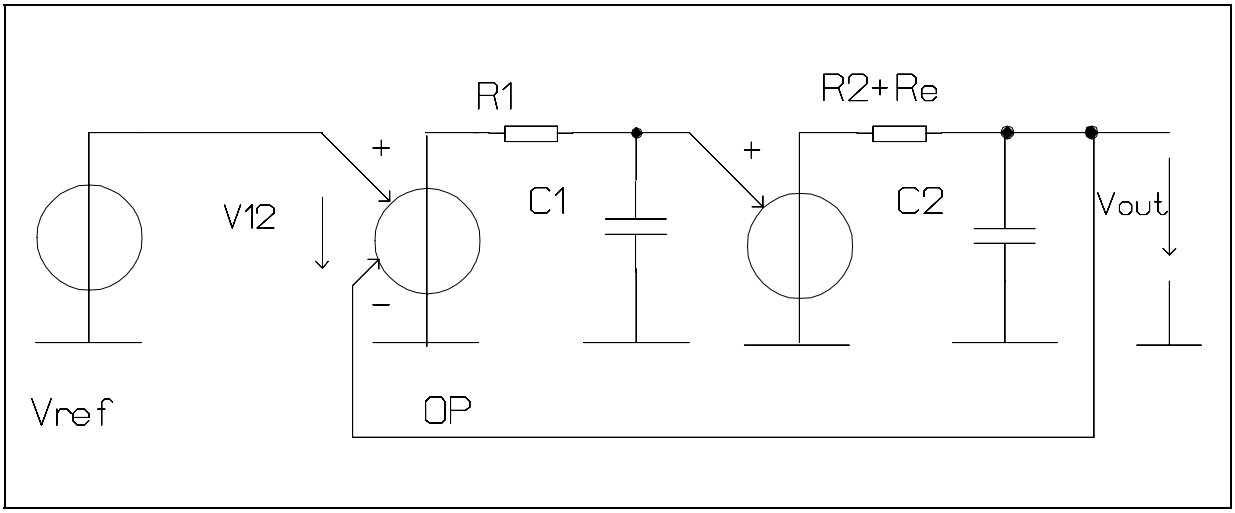


Figure 2: Representation of the Topology of Fig. 2 by Voltage Controled Voltage Sources



The operational amplifier can be described as a voltage controlled voltage source and a low pass filter. The control voltage is nothing else than the difference between the reference voltage and the divided output voltage. The output stage consists of a darlington emitter follower which can roughly be modelled as a follower stage with a voltage gain of one and an output impedance of two times Vt divided by the output current plus the current sense resistor. Fig 2 shows this representation.

Let us see the behaviour of this kind of regulator. The DC performance is defined by the output impedance R2 (R2 is the current sensing resistor use for the short circuit protection) in series with the emitter impedance of the output transistor Re (Supposing the load resistance is much higher than R2 and Re it is neglected) and the DC gain K of the operational amplifier (usually several hundred to some thousand).

$$Vout = Vref + V12 \cdot K - (R2+Re) \cdot Iout \qquad (2.1)$$

In this equation the deviation of the output voltage V12 can be derived. This Yields

$$\frac{dV12}{dIout} = \frac{(R2 + Re)}{K} \qquad (2.2)$$

Equation (2.2) describes the DC output resistance of the voltage regulator. The frequency response of the operational amplifier is modelled by R1 and C1. Approaching the gain bandwidth product of the operational amplifier K becomes one and the output impedance of the whole regulator is mainly determined by R2 and Re. The value normally is in the range of one Ohm or even less. So the cut-off frequency of the output impedance and the external capacitor C2 becomes

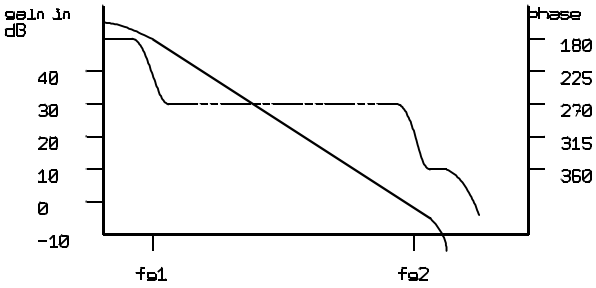
$$fg2 = \frac{1}{2\pi\,(R2 + Re)\,C2} \qquad (2.3)$$

Assuming C2 around 100 nF, fg2 is in the range of several hundred kilohertz. So R1 and C1 are designed to become the first pole reducing the loop gain to less than one at fg2.

$$fg1 = fg2 / K \qquad (2.4)$$

Fig 3 shows the typical open loop gain and phase curves of the regulator.

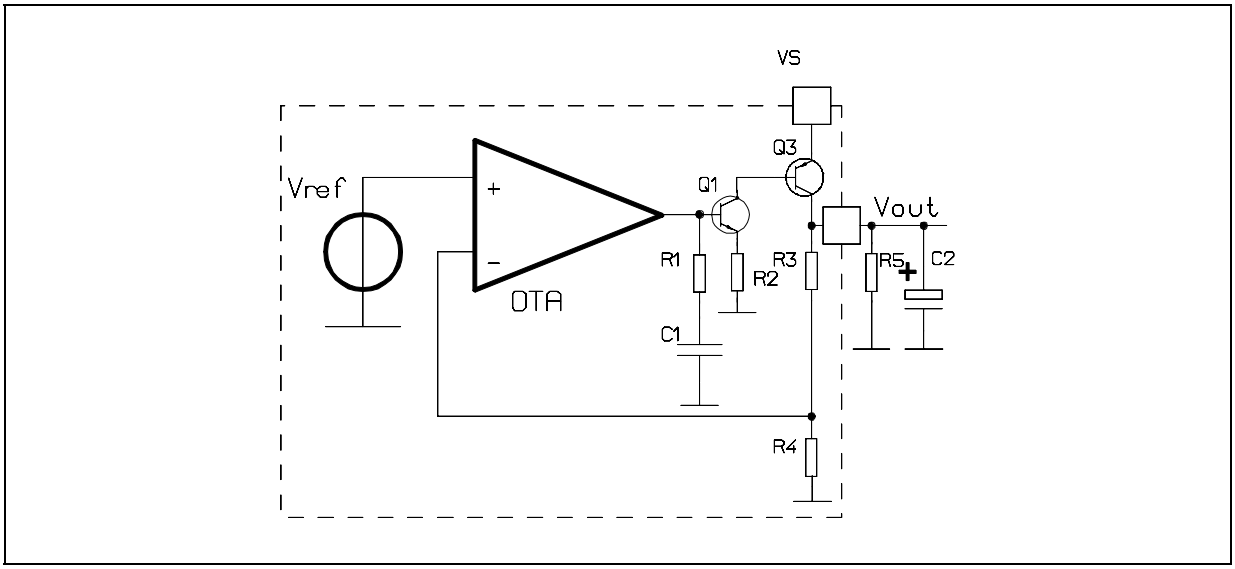
Figure 3.



The gain becomes less than one before the second pole shifts the phase an other 90 degrees. When the total phase becomes (including phase inversion of the regulator itself) 360 degree the gain must be less than 0 decibel (corresponding a loop gain of one) to provide stability.

This kind of regulator is quite economical and robust. The drawback is the voltage drop between input and output of the device. To keep up regulator function two Vbe plus a certain headroom for the operational amplifier is required. This adds up to about two volt at low temperature!

Figure 4: Very Low Drop Regulator



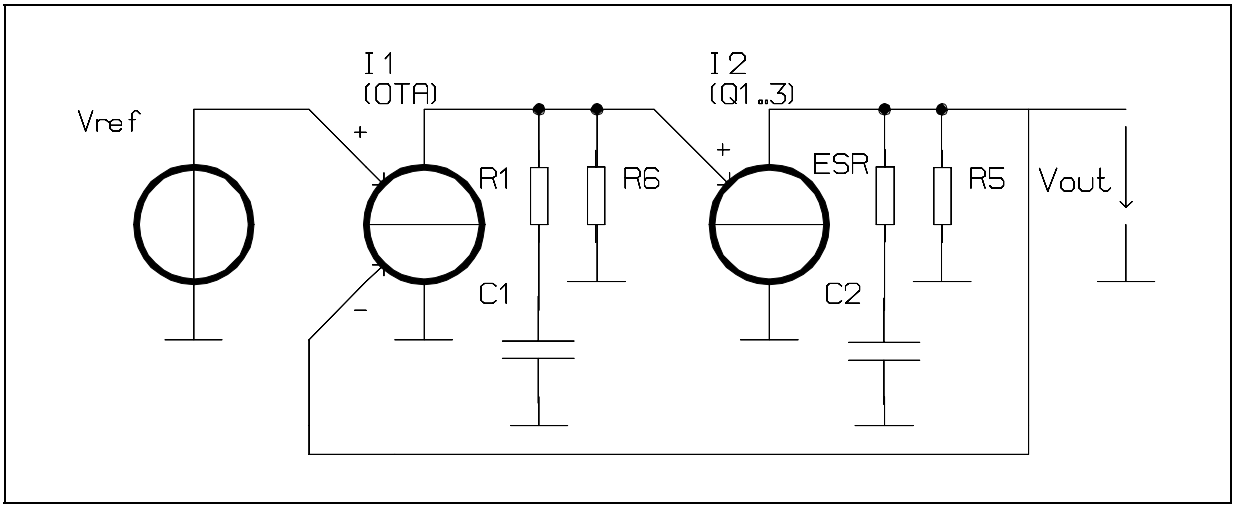
3. THE VERY LOW DROP REGULATOR

To overcome the voltage drop restriction of the standard topology very low drop regulators have been introduced. The very low drop regulator uses a PNP transistor in it's power stage. So the drop required for proper function falls downto the saturation voltage of this PNP transistor, which is in the range of some hundred millivolts. Fig 4 shows the topology of such a very low drop regulator including it's load and external capacitors.

Here the output is driven by a collector. So the stage consisting of Q1 and Q3 can be represented by a voltage controlled current source. The output current is transformed into an output voltage by integrating this current with C2. The control voltage is the base voltage of Q1. Normally Q1 is a darlington transistor in this kind of circuit. As it is easier to implement in integrated circuits, the amplifier OP usually is built as an an operational transconductance amplifier. This yields the idealized circuit shown in fig. 5.

I1 is the operational transconductance amplifier mentioned above. As the voltage divider of the feedback loop is omitted the reference voltage Vref now becomes the equal to the desired output voltage. (The voltage divider found in most regulators just introduces a constant factor into the loop.) I2 represents the output stage consisting of Q1..Q3. R6 represents the input resistance of the second stage. So the integrated circuit converts a deviation between the output voltage and the reference voltage into an output current. To make an output voltage of this current the integrating behaviour of C2 is mandatory. This automatically makes the external capacitor together with the

Figure 5: Representation of a Very Low Drop Regulator by Voltage Controled Current Sources



load impedance R5 define the first pole! This is a completely different situation compared to the standard voltage regulator described in paragraph two. Of course C2 being an electrolytic capacitor is far from making it an ideal integrator. The effective series resistance ESR already becomes dominant at considerably low frequencies around some hundred Herz. The first cut-off frequency where the integrating behaviour of the loop begins, can be calculated by:

$$fg1 = 1 / 2 \pi R5 C2 \qquad (3.1)$$

At fg2 the effective series resistance becomes dominant devaluating the integrator again. Equation (3.2) yields this frequency.

$$fg2 = 1 / 2 \pi C2 ESR \qquad (3.2)$$

At fg2 the loop gain is still much higher than one. To maintain stability, a well defined second low pass must reduce the gain downto one before further phase shifters add an other 90 degrees causing instability. (Example: Supposing Your application can tolerate an output voltage change of 20 mV at a load change of 400 mA the required transconductance of the complete regulator can be calculated.

$$S12 = 400 mA / 20 mV = 20 A/V$$

With an ESR of one ohm this yields a loop gain of

$$gain = S12 \cdot ESR = 20$$

(or 26 in decibel.) A good choice is making fg2 the cut-off frequency of the chip internal frequency compensation. So C1 becomes

$$C1 = 1 / 2 \pi R6 fg2 \qquad (3.3)$$

With

$$R6 = B \cdot R2 \qquad (3.4)$$

where R2 is the emitter resistor of figure 4 and B the gain of the driver transistor Q1. To keep C1 in a feasible range, Q1 usually has to be a darlington transistor. At a certain frequency, let us call it fg3, further parasitic poles become a matter of concern. There the phase shift of the low pass C1 should decrease. (This frequency is determined by chip internal propagation delays. These delays may be quite significant in low consumption devices requiring extremely high internal impedances while pocket capacities even increase due to large resistors. Reducing the pocket capacities associated with the pocket size isn't possible because the device might have to handle a wide supply voltage range.) This yields the value for resistor R1.

$$R1 = 1 / 2 \cdot \pi \cdot C1 \cdot fg3 \qquad (3.5)$$

If fg3 is determined by multiple parasitic poles the loop gain must under all circumstances be less than one at this frequency. Then a maximum value for the tolerable ESR is given by:

$$ESRmax = fg3 / S12max \cdot fg2 \qquad (3.6)$$

with fg2 according to the internal compensation described by equations (3.3) and (3.4). If fg3 is only determined by a single parasitic pole the situation becomes a little more relaxed. Fig 6 shows a bode plot of the cut open loop of such a very low drop regulator with multiple parasitic poles representing the worst case in an application, where the external pole is exactly fitted with the internal (on chip) frequency compensation.

Fig. 6 shows the ideal case of solving equation (3.2) and (3.3) giving the same frequency fg2. This is not always the case. Depending on the practical value of the effective series resistance equation (3.2) and equation (3.3) may give different frequencies for fg2. Supposing an ESR less than ESRmax we obtain a bode plot similar to fig. 7.

Figure 6.

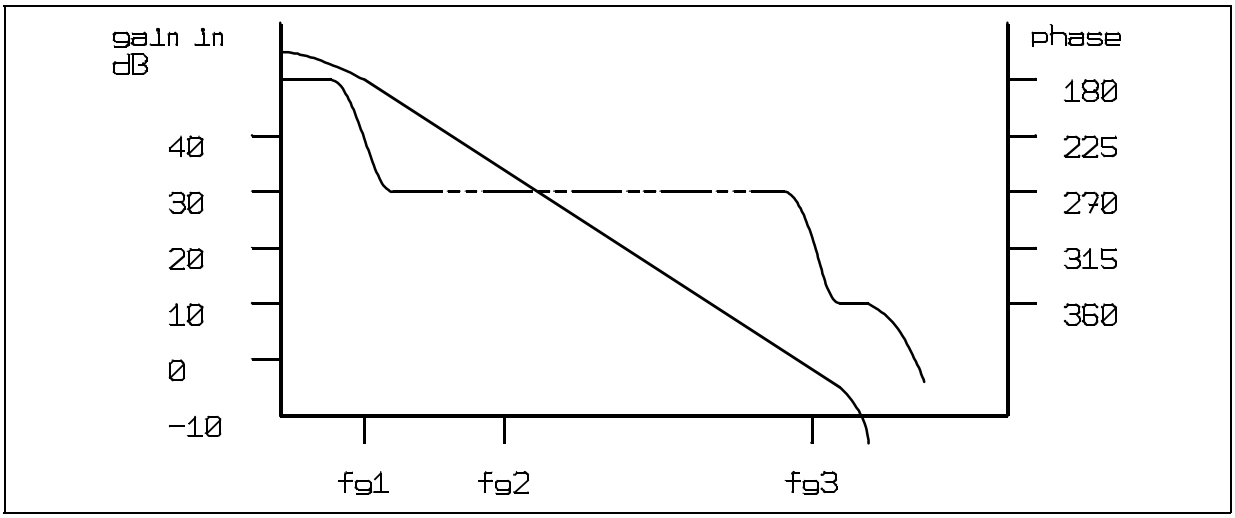


Figure 7.

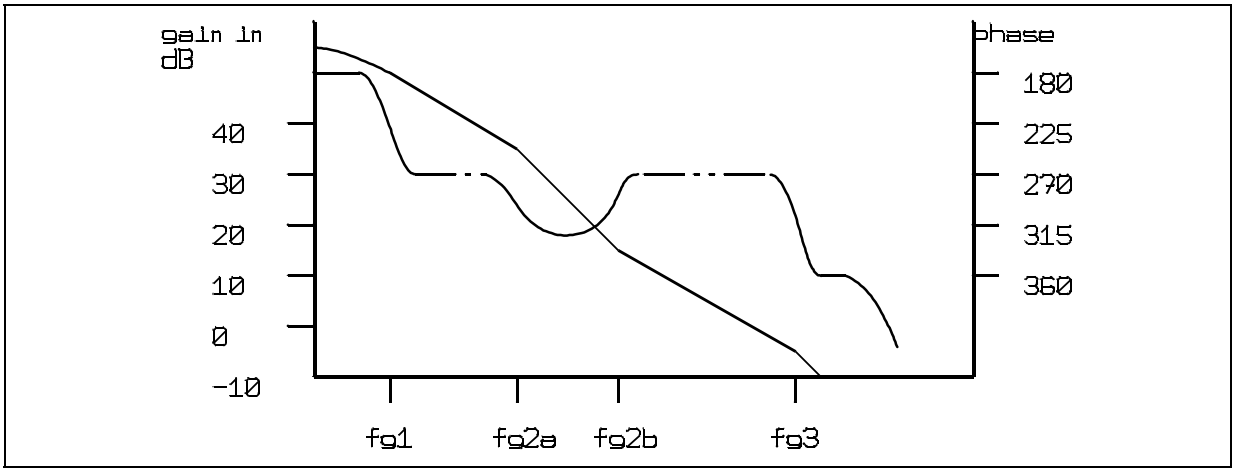
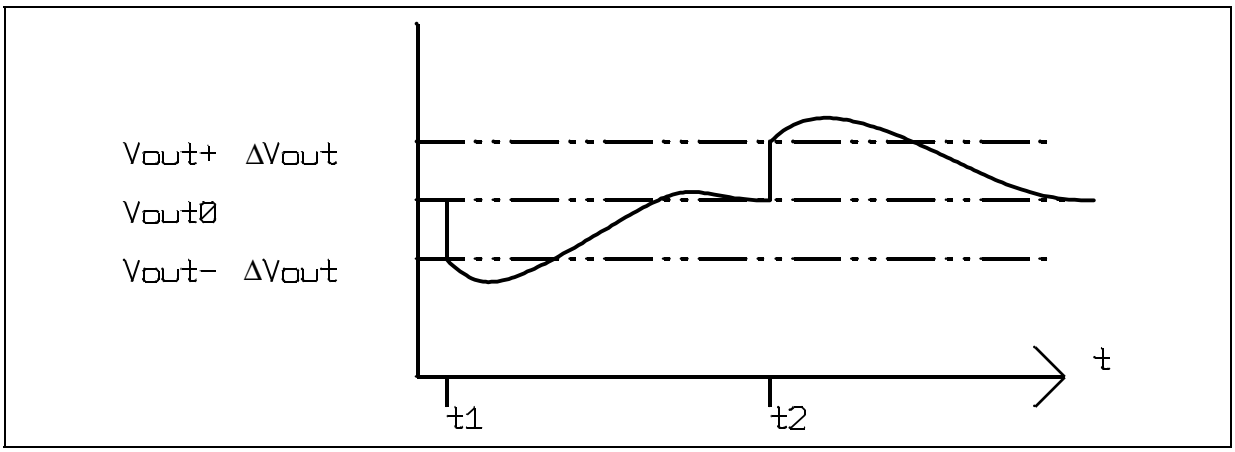


Figure 8.



Here the phase margin approaches zero degrees between fg2a and fg2b. Fortunately the two integrators involved (external capacitor C2 and internal capacitor C1) are degraded by the series resistors R1 and the ESR. So analytic calculation omitting approximations show that the loop will stay stable. Nevertheless the regulator will tend to ring if the effective series resistance ESR becomes too small. As the charge and discharge currents of C2 are limited the ringing signal may become triangular shaped in many applications.

3.1 Reaction on Load Transients

We have seen the bode plots of standard regulator topologies and very low drop topologies differ a lot. Let us now investigate the reaction on load changes. An abrupt increase of the load current will have to be satisfied by the output capacitor (C2 in fig. 5) first because the collector of the power PNP transistor will in the beginning act as a current source providing just the same current as before the load change. Due to the ESR of this capacitor the output voltage will drop immediately. Equation (3.1.1) calculates this impact.

$$\Delta Vout = ESR\ \Delta Iout \qquad (3.1.1)$$

Then the capacitor will be discharged until the regulator reacts. The initial slope is defined by:

$$\frac{dVout}{dt} = -\frac{\Delta Iout}{C2} \qquad (3.1.2)$$

Abrupt reduction of the load current will have a similar effect. First the output voltage increases immediately according to equation (3.1.1) again. Then C2 will be charged. Equation (3.1.2) describes this if ΔIout is inserted with a negative sign. After this overshot the regulator will turn off and the capacitor C2 will be discharged again by the reduced load current. Again equation (3.1.2) can be used. Keep in mind very low load currents after an abrupt change will lead to a long time constant of the overshot! Fig. 8 illustrates this behaviour.

3.2. Reaction to Supply Voltage Transients

The reaction to supply voltage transients is depending much on details of the circuit of the regulator. In general low consumption devices tend to be more sensitive because high internal impedances together with the technology dependant (and so they are supply voltage dependant!) pocket capacities need more time to recover from transients. Nevertheless some optimisation can be achieved by smart design.

Designs using integrated prestabilisation circuits to supply the high performance reference and regulator blocks may lead to almost transient immune circuits! The standard L4938 family already uses a simple prestabilization guaranteeing good transient performance at a supply voltage range from 7V to 40V. The prestabilisation is straight forward using a low precision bandgap that is only optimised for transient robustness. The precision reference is generated in a second bandgap that is optimised for high accuracy. Although this is an easy to understand design this prestabiliser has certain limitations:

Supplying everything from the input the device still is prone to negative supply transients (below 7V). The independant prestabilising bandgap consumes an additional supply current of about 40µA which could not be tolerated for extreme low consumption applications.

The L4938E family uses a new approach to solve the disadvantages of the independant bandgap prestabilisers. Some Vbe are added to the reference voltage. This is used as the bias of the prestabiliser. Additionally the prestabiliser has a second supply path from the output OUT1. In fact as soon as the output voltage (at OUT1) is high enough all the internal circuitry of L4938E is supplied by OUT1. The supply path from VS is only required to start the device. So transients on VS will not harm the performance as long as the supply pin doesn't go below 2V (which is required by the starter).

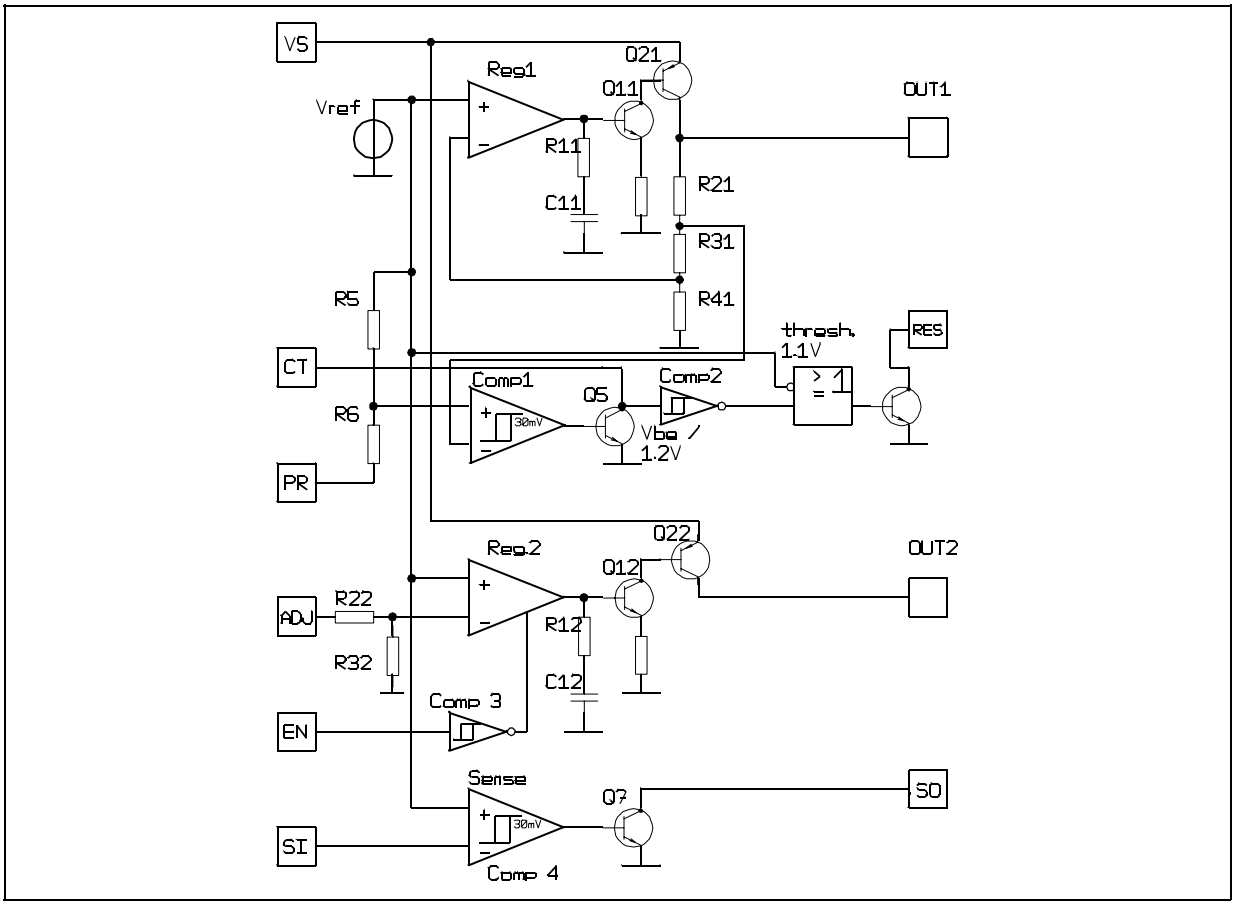
Of course during the time the input voltage is less than the desired output voltage the load has to be supplied by the output capacitor.

4. THE L4938E FAMILY IN DETAIL

As we have been entering into circuit specific characteristics let us see the schematic of the L4938E family .

The two voltage regulators Reg1 and Reg2 are of

Figure 9



the very low drop kind discussed before. Regulator1 is permanently active. Regulator2 can be enabled by a logic LOW at input EN. If Reg.2 is disabled the total current consumption of the L4938E is 70µA (typically) plus the base current of Q21, which is 1/40 th of the load current.

4.1. Regulator 1

Regulator 1 is capable of supplying loads up to 100mA. The effective series resistance of the external capacitor (See Fig 5) C2 should be less than 5Ω. The capacity should be more than 10µF. In most applications external capacitors (C2 in Fig. 4) around 22µF are to be expected. The load (R5 in Fig. 4) will range from several KΩ down to 50 Ω. Supposing a load of 500 Ω and an effective series resistance of one ohm the first (almost) integration will start at:

$fg1 = 1/2\,\pi \cdot 22\,\mu F \cdot 500\Omega = 14.5\ Hz$ (see Eq. 3.1)

and end at:

$fg2b = 1/2\,\pi \cdot 22\mu F \cdot 1\Omega = 7.2KHz$ (see Eq. 3.2)

In Reg.1 the base impedance of Q11 (which actually is a darlington transistor) represented by R6 of Fig 5 is approximately 3.5 MΩ. Consequently the second integrator with a capacity of 33 pF will take over at

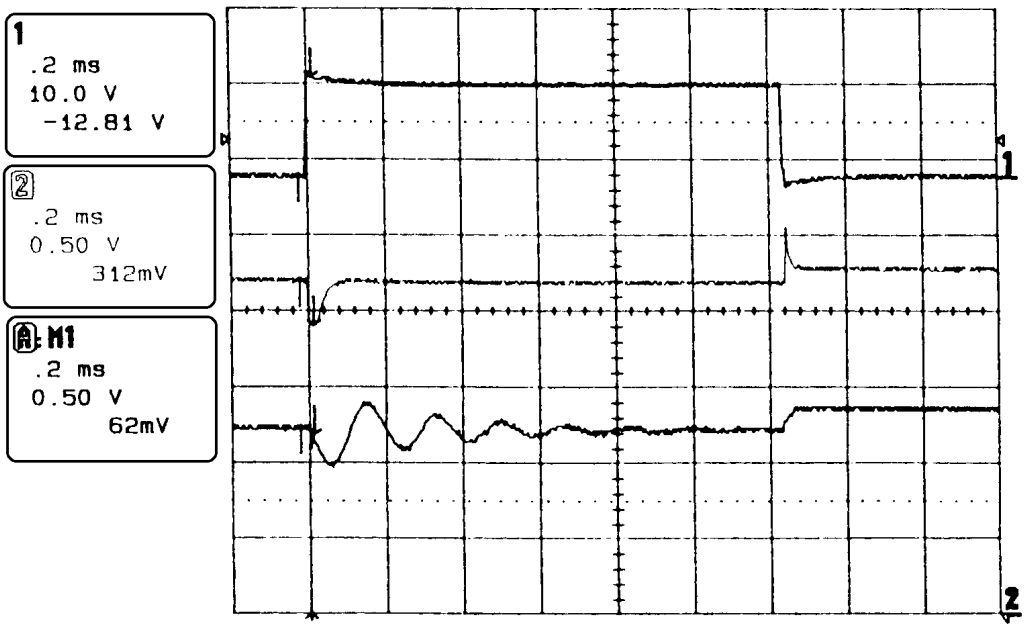
$fg2a = 1.4\ KHz$

This is the optimised value for a worst case ESR of 5Ω. So we find two almost integrating low pass filters between 1.4 KHz and 7.2 KHz. Fortunately they both are damped and shift phase by slightly less than 90 deg. each thus keeping the loop stable. Nevertheless using extremely low ESR values the loop will (As all very low drop regulators do) tend to ring after transients. With ESR values of more than some tenth of an ohm ringing will already disapear (ESR values approaching zero correspond to a low fg2a in figure 7). In this frequency range some phase margin has to be sacrificed in favour of leaving margin for higher ESR values. Beyond 70 KHz parasitic capacities inside the regulating amplifier begin to act as a further single order pole. Therefore R1 devaluates the integrator C1 at:

$fg3 = 1/2\,\pi \cdot 33pF \cdot 70K\Omega = 69KHz$

keeping the phase margin until further poles make the amplifier more and more behave like a delay line above 200 KHz. Fig 10 shows the response of the regulator to load changes.

Figure 10: Response of the regulator to load changes.



Top trace:	Drive of load transistor. HIGH correspond 100Ω. LOW corresponds no load.
Middle trace	Response with 10µF, ESR = 4.7Ω; 0.5V/division.
Bottom trace	Response with 10µF, ESR approaching 0; 0.5V/division

Figure 11: Temperature dependence of the output voltage of OUT1

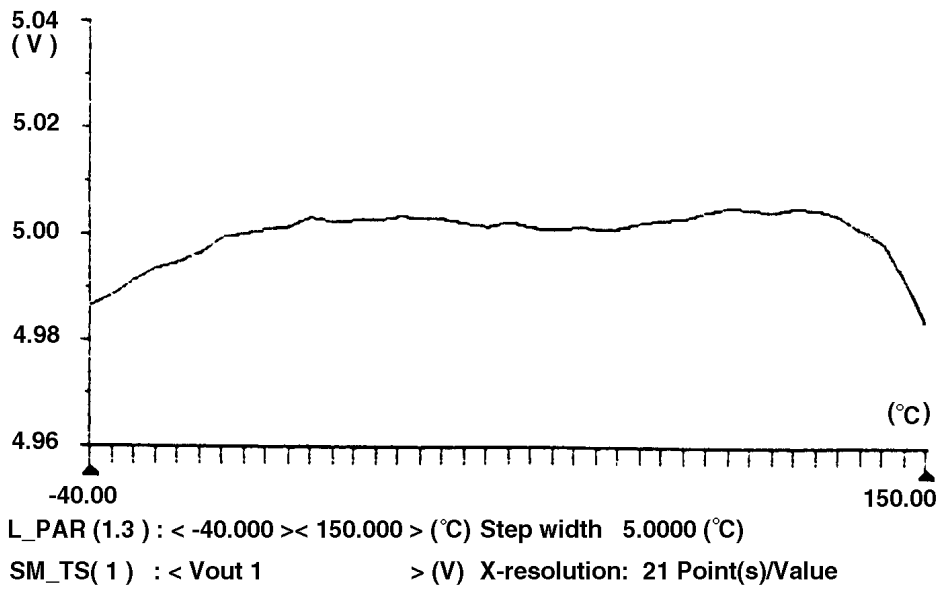
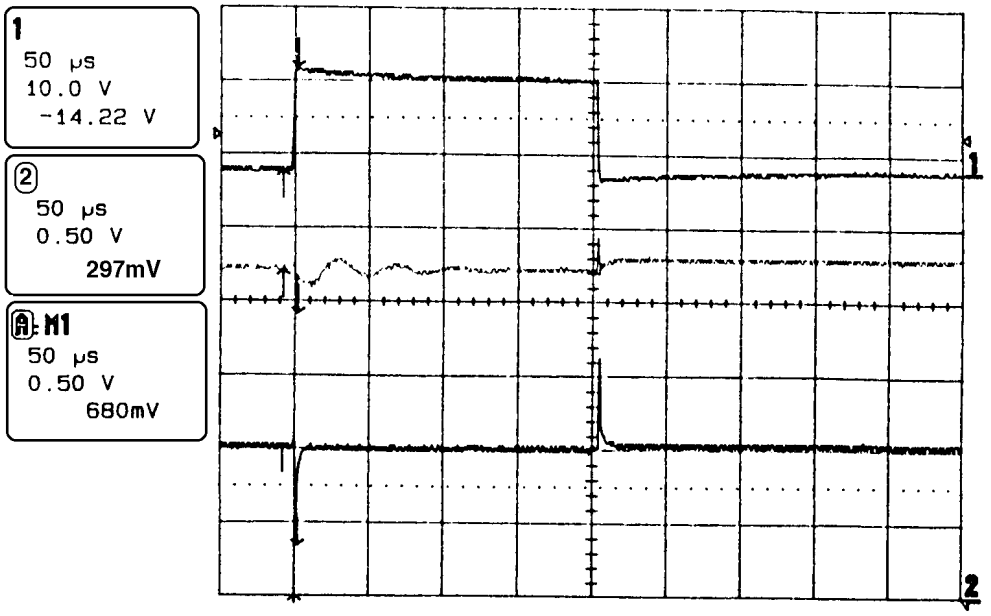


Figure 12: Response to the load changes.



Top trace:	Drive of load transistor. HIGH correspond 100Ω load. LOW corresponds no load.
Middle trace:	Response with 10µF, ESR approaching zero (Plastic capacitor); 0.5V/division.
Bottom trace:	Response with 10µF, ESR = 4.7Ω; 0.5V/division

The regulator is committed to high precision using state of the art circuitry cancelling base currents by dummy transistors and cancelling leakages by symmetrizing the circuit with dummy leakage generators. Fig 11 shows the result of these efforts.

The regulator is of course protected against overload and against over temperature. Thermal shut down of regulator 1 takes place at a 10 K higher temperature than thermal shut down of regulator 2. So in critical application the output of regulator 2 can be monitored as a prealarm before regulator 1 shuts down too. The thermal shut down is an analogue one regulating down the output voltage until power dissipation inside the chip and the thermal conduction balance.

4.2 Regulator 2

Regulator 2 is designed very similar to regulator 1. Besides the features of regulator 1 regulator 2 can be disabled by a logic HIGH at pin EN. This reduces current consumption significantly. (Stand by consumption specified in the data sheet is refered to regulator 2 being disabled.) As this regulator has to provide more current than regulator 1 all internal impedances and current densities are scaled according to the higher maximum output current. So all parasitic cut-off frequencies shifted higher and frequency compensation had to be designed different. Cut-off frequency fg3 has been found at

fg3 = 190 KHz

This allows choosing the cut-off frequency fg2 at 7 KHz. So regulator 2 will recover faster from load transients. Fig 12 shows the response to load changes.

Like regulator 1 regulator 2 is optimised for maximum accuracy. Regulator 2 has a thermal shut down. This shut down takes place before regulator 1 turns off.

4.3 The Reset Circuit

The reset circuit consists of three major parts. Comp 1 supervises the output voltage of OUT1. The external capacitor, that may be connected to pin CT together with Comp 2 provides a well defined minimum reset pulse width. The OR gate between Comp 2 and Q6 supervises the bandgap voltage forcing RES LOW as soon as the reference breaks down corrupting the operation of Comp 1.

4.3.1 The Reset Path via the Comparators

Comp 1 compares the divided output voltage with the reference inside the circuit. Pin PR left open the reset threshold is typically 300 mV below the nominal output voltage. To alter the reset threshold pin PR can be connected to ground via a resistor or even be shorted to ground. By this measure the reset threshold can be programmed between typically 3.8V and 4.7V . The resulting threshold can be calculated by

$$V_{res} = \frac{4.7V \cdot (R_{PR} + R6)}{R_{PR} + R5 + R6} \qquad (4.3.1)$$

With R_{PR} being the external resistor
R5 = 20KΩ and R6 = 80KΩ, R5 and R6 are matched but have an absolute tolerance of 20%.

If Vout1 falls below the reset threshold, Q5 discharges the capacitor at pin CT. The pull down current ICT is between 3 mA (at -40 deg. C) and 15 mA (at 150 deg. C). Consequently the reset is delayed depending on the capacitor at CT.

$trr = 3V \cdot CT / ICT + t_{rr0}$ (4.3.2)

t_{rr0} is the propagation delay of the reset circuit without capacitor.
t_{rr0} is around 15 µs

As soon as VCT drops below Vbe the logic output RES becomes LOW. It will remain LOW until the voltage at CT reaches 1.4V again. The minimum reset time is

$t_{RDmin} = (1.4V - Vbe) \cdot CT / 1\mu A$ (4.3.3)

depending on the junction temperature Vbe ranges from 0.2V to 0.7V

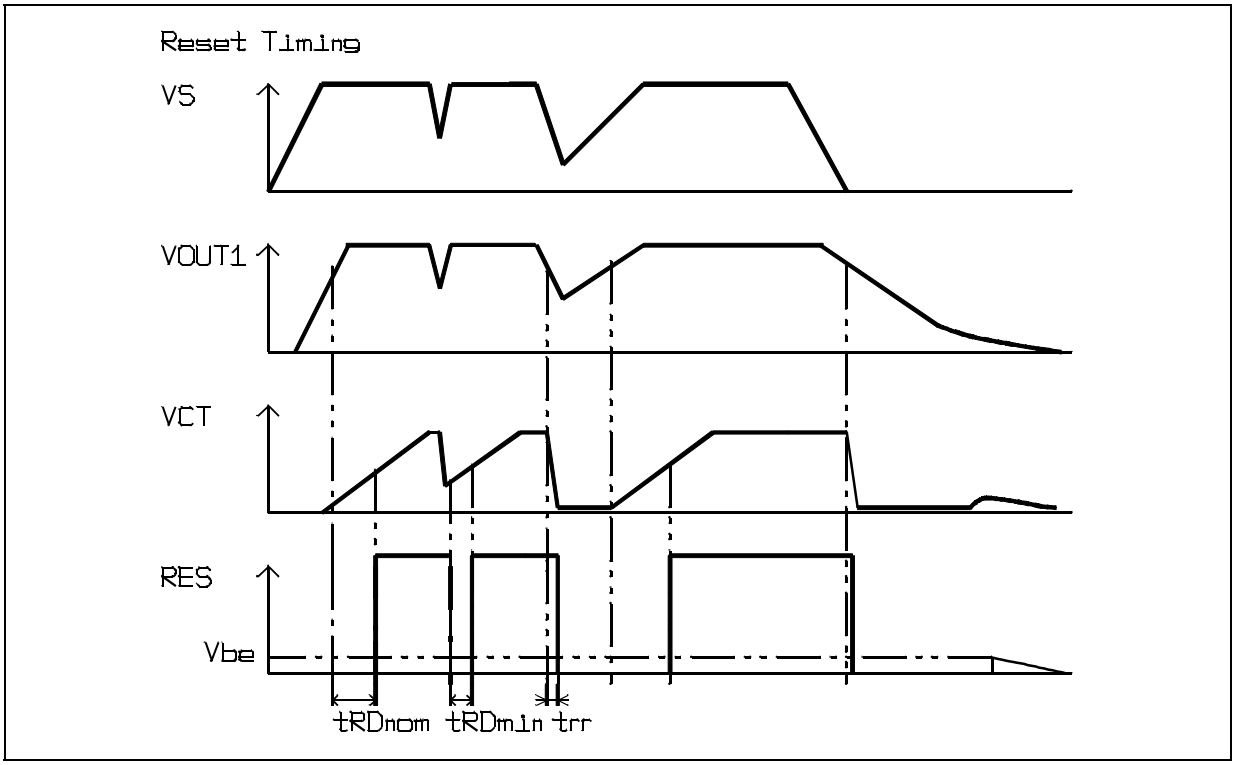
This minimum time reset will only take place after extremely short impacts on the output that does not allow full discharge of CT. Normally CT will be discharged downto the saturation voltage of Q5. The nominal reset delay then becomes

$t_{RDnom} = (1.4V - Vsat) \cdot CT / 1\mu A$ (4.3.4)

Vsat is always around some millivolts.

t_{RD} always starts at the time the output has recovered again. Fig 13 shows a typical timing of the reset circuit.

Figure 13.



4.3.2 The Default Reset Path

Of course functionality of this reset circuit requires a correct bandgap voltage reference. But the bandgap reference being an enhanced precision circuit incorporates cascode amplifier stages avoiding early effects. Therefore depending on temperature it requires a certain supply voltage (min $V_{BG} + 3 \cdot V_{be} + 2 \cdot V_{sat} = 3.5V$ at ambient temperature). Without controlling the bandgap voltage, a race between the supervised output voltage and the reference voltage could occur if the bandgap supply (that is taken from VS or OUT1 whatever is available) falls below a certain level. Consequently the input of the OR gate between Comp 2 and Q6 checks the bandgap circuit for a correct reference value. If the bandgap voltage is found to be too low a LOW at output RES is initiated without caring for any conditions met at pin CT. The OR gate driving Q6 is supplied from OUT 1. So the LOW at RES can be held until OUT1 drops below V_{be}. This feature is a must in modern microprocessor systems. Imagine what would happen if your microprocessor changes the system EEPROM during the last maybe three volts of the falling slope of the supply voltage just because the reset has become HIGH again which could happen with some older reset circuits. The whole reset circuit is always active. It is not turned off in stand by mode (EN HIGH).

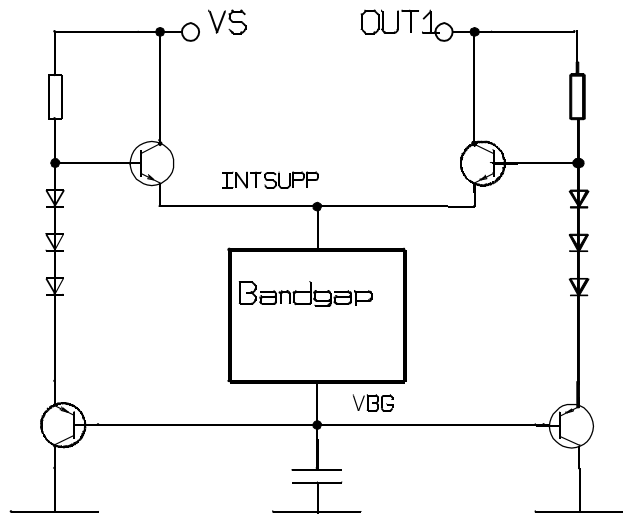
4.4 Comparator Comp 4

Comp 4 is an uncommitted comparator for example to be used to generate an alarm before reset occurs when the supply VS is turned off. The bandgap voltage is used as its reference. Due to the drive current of Q7 the comparator cunsumes more current if input SI is LOW (V_{SI} 1.23V). Like the reset circuit the comparator is permanently active, but it has no default path activated by bandgap fails.

5 EMI CONSIDERATIONS

Although it is a low current consumption device the L4938E is optimised for rough automotive environment. Special care was taken to make it insensitive to supply transients and input transients at EN and SI.

Figure 14: Simplified Presabilization

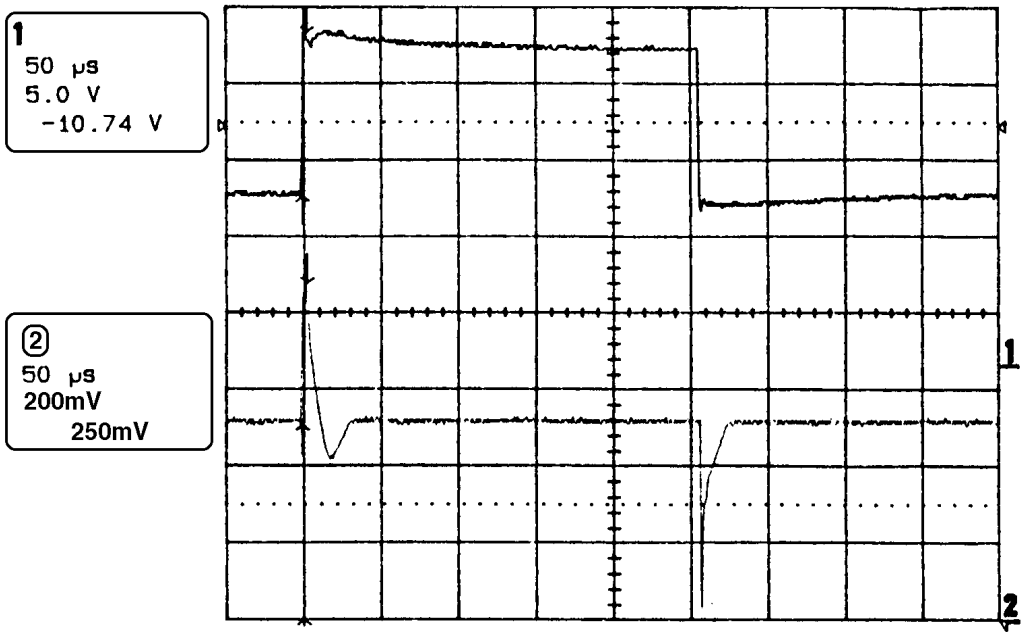


5.1 Protection of the Internal Reference Voltage Generator

The bandgap being the heart of the L4938E is supplied by an internally prestabilized rail. Fig 14 shows the simplified prestabilization.

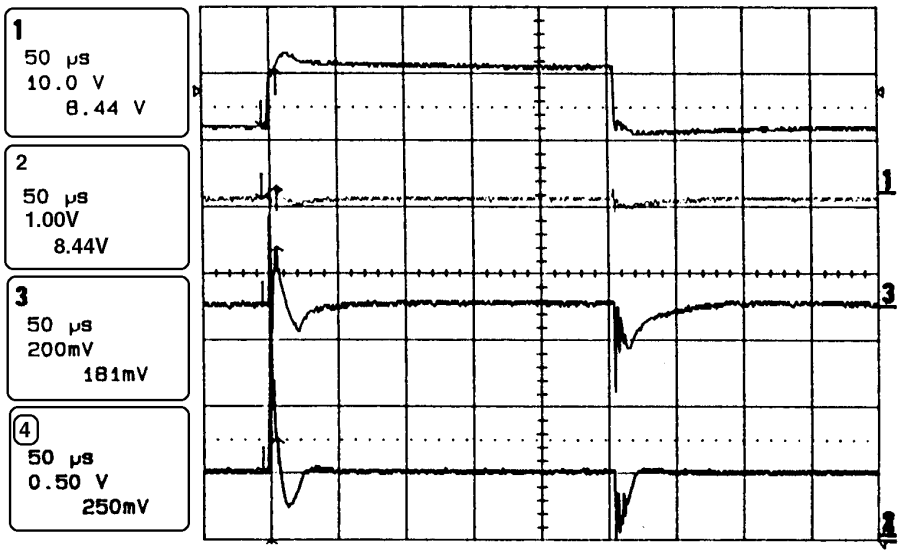
Transients at VS will only have little influence on the bandgap voltage. This can be measured at pin PR if it is left open. Fig 15 shows the pulse response of the bandgap together with the prestabilization.

Figure 15: Supply transient response of the bandgap reference circuit.



Top trace: Supply voltage; 5V/division
Bottom trace: Response transient response; 200mV/division. (Measured at pin PR)

Figure 16: Supply transient response of the voltage regulators and reset circuit.



Top trace:	Supply voltage; 20V/division
Second trace:	Reset output connected to OUT1 via 10KΩ (no reset fail).
Third trace:	OUT1; 0.2V/div. Load = 100Ω
Bottom trace:	OUT2; 0.5V/div. Load = 33Ω

5.2 Voltage Regulators

Like the bandgap the regulating amplifiers are supplied by an internal rail. So their response to supply transients is quite moderate as can be seen on Fig. 16 .

Injecting RF into sensitive feed back loops can lead to malfunction of the regulators if certain values are exceeded. Actually the outputs OUT1 and OUT2 and feedback input ADJ should be kept free from RF. Between OUT2 and ADJ there should be no low pass because this would shift the phase of the regulation loop. This reduces stability of the loop or could even cause oscillation. The best solution is blocking the outputs with an SMD ceramic capacitor connected to ground as near to the circuit as possible.

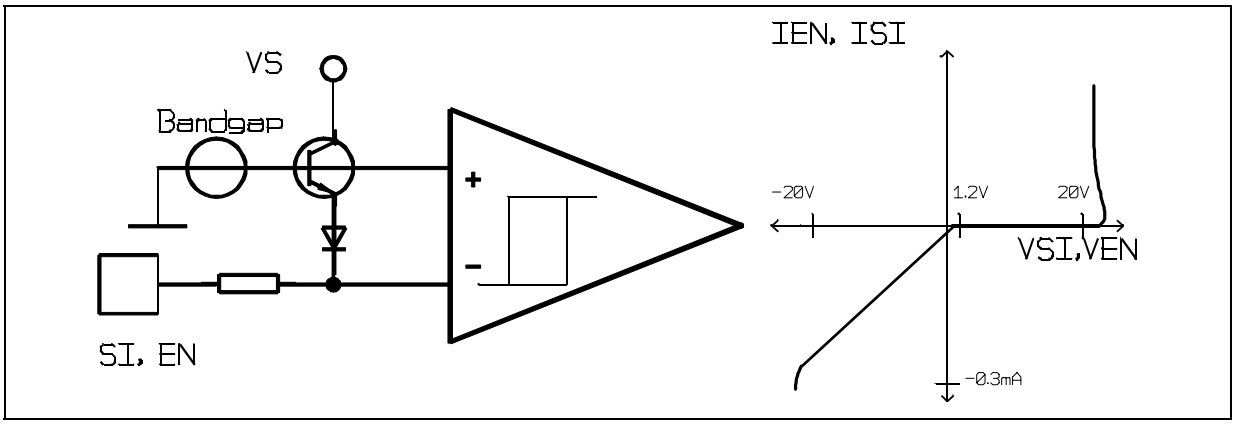
5.3 Reset Circuit

To make reset insensitive it is supplied by the internally presabilized rail too (except the drive of Q6). To make the default path insensible too an on chip delay of approximately 20µs is implemented. Even without the use of an external delay capacitor at pin CT reset has become very robust. This can be seen on Fig. 16 too. The pins CT and RES being open collectors incorporate a lateral NPN transistor that will be activated if one of those pin is dragged below $-V_{be}$. If this unavoidable parasitic is activated it can cause unexpected results in other parts of the circuit. To keep antennas inefficient the capacitor at CT should be connected with short wires. As leakages in SMD ceramic capacitors were reported we recommend the use of a foil capacitor. Output RES is suited to drive logic devices on the same board as the L4938E . Long wires or wires leaving the board may therefore require RF blocking means. Pin PR is directly connected to the bandgap that is the heart of the circuit. So this pin should either be connected to a resistor to ground using the shortest possible way (small antenna loop) or left open. Dangling wires connected to PR could act as an antenna and therefore are to be avoided.

5.4 Sense Comparator and Enable Input

In automotive applications ground bounce of several volts is quite common. So the inputs EN and SI are hardened against negative input pulse downto -20V by a special protection structure. Besides the protection this structure acts as a low pass too. Fig 17 shows the simplified schematic of this protection and the resulting input characteristic.

Figure 17: EN, SI negative transient protection.



The comparators Comp 3 and Comp 4 have reaction times of several microseconds to make the insensible to short transients. Like RES the sense output SO is an open collector topology and should not be reverse polarised.

5.5 Reverse Supply Protection.

The supply voltage may be reverse polarised to -14V without destroying the device. Of course it doesn't work anymore then. Even during reverse supply condition the outputs OUT1 and OUT2 remain at a minimum voltage of $-V_{be}$ because the power transistors are turned off then. Components supplied by the L4938E under normal circumstances will not be harmed.

6. SPECIAL APPLICATION CONSIDERATIONS

Having become aware that very low drop voltage regulators require some care about effective series resistances of the output capacitors and about harsh load transients there should not be many problems left in standard applications. Nevertheless let us have a look at some maybe less typical circuits.

6.1 Using OUT2 as a High Side Switch

Sometimes only one 5V supply and a high side switch is needed in an electronic system. This typically is the case if a microprocessor is working together with interface circuits that may be operated throughout the whole voltage range of the system supply (VS of the L4938E). Here it becomes a very attractive solution to use OUT2 of the L4938E as a high side switch turning on the supply of the interface circuits as soon as the system changes from stand by to operation. So the system will work with a low stand by consumption even if the interface circuits require a certain supply current (because the supply of the interface circuits will be turned off in stand by mode). For such applications pin ADJ only has to be disconnected from OUT2 (leaving pin ADJ open or shorting it to ground will yield the same behaviour). Now regulator 2 will be driven into dropout operation as soon as it is enabled (EN=LOW). With an opened regulation loop the output capacitor of OUT2 is not required for stability anymore. Nevertheless we recommend a certain capacity to avoid undershots of OUT2. Two conditions however should be considered carefully.

Supply voltage range: As the loop is cut open OUT2 will just follow the supply VS. The ESD protections of OUT2 are suited for a maximum output voltage of 20V. Therefore operation with supply voltages higher than 20V using the regulator as a high side switch may be destructive for the protections of OUT2 (Because the ESD protection at OUT2 could ignit and keep conducting at a high current for a longer time than it is suited for.).

Inductive loads: Inductive loads such as long wires or inductors may cause an undershot of OUT2 at turn off. Undershots below -VBE at OUT2 activate parasitic components and must be avoided under all circumstances. Appropriate means to avoid such undershots are clamps using shottky diodes or an output capacitor fulfilling equation (6.1.1) .

$$C_{OUT2} > L \cdot I^2/V^2_{OUT2} \qquad (6.1.1)$$

C_{COUT2} is the capacity attached to OUT2
L is the inductivity of the load
I is maximum current flowing before turning off the switch V_{OUT2} is the minimum voltage C_{OUT2} is charged to before the switch turns off.

6.2. Paralleling of Outputs

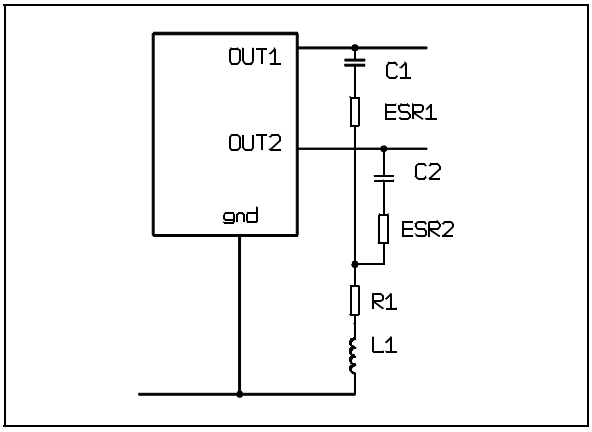
If both outputs are paralleled the different regulation loops may interfere with each other. This may lead to instability although each regulator individually is stable. (Some single poles of the two regulators are realtively close. Depending on load conditions paralleling the regulators may lead to

pole splitting converting two poles on the real axis into a complex pair of poles.) Paralleling of outputs should not be done for this reason. If this can not be avoided due to specific conditions of an application the outputs at least should be decoupled by a resistance of some ohm or by a diode. Stability in such applications should be investigated by the user very carefully.

6.2.1 Long Common Ground Wires for Both Output Capacitors

Connecting the ground node of the output capacitors to ground far away from the regulator can lead to the same situation as paralleling the outputs because there will be an AC short circuit between OUT1 and OUT2. This is illustrated by Fig. 18.

Figure 18: Equivalent Circuit of Long Common Ground Wires



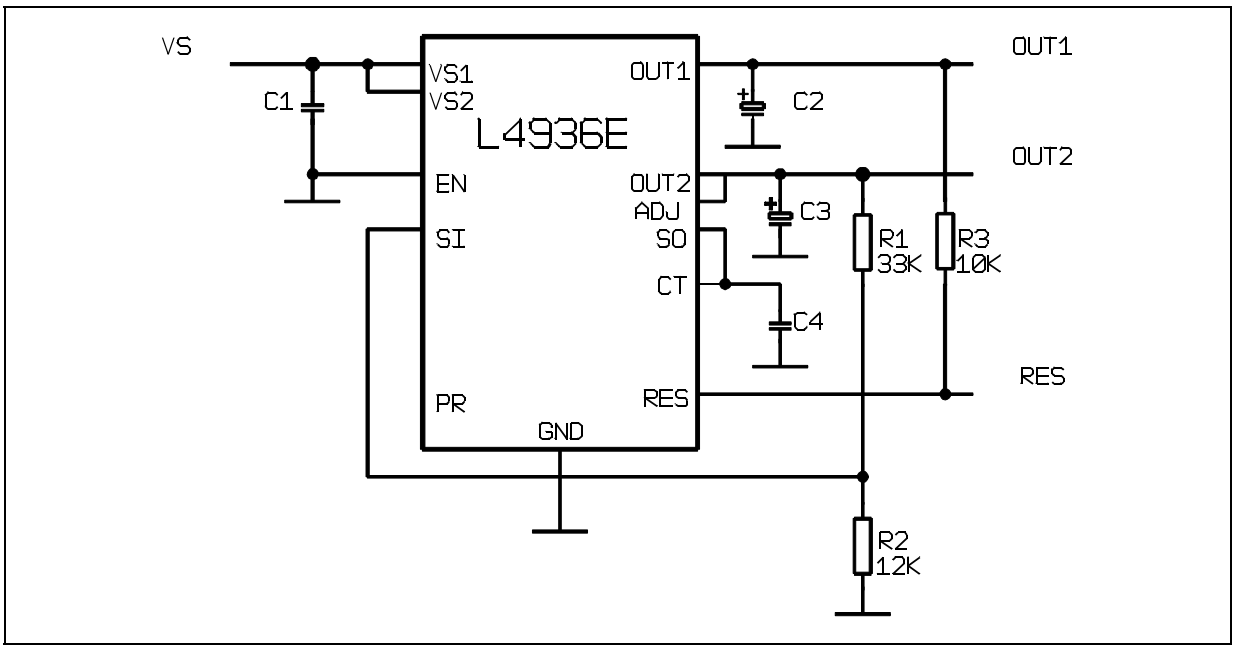
Here C1 together with ESR1 represents the output capacitor of regulator1 while C2 together with ESR2 represents the output capacitor of regulator2. R1 is the resistance and L1 the inductivity of the ground wire between the common ground node of C1 and C2 and the ground node of the voltage regulator. If the effective series resistances ESR1 and ESR2 become small compared to R1 and the AC impedance of L1 the output capacitors act as AC short circuits between the outputs. So the output capacitors should be connected to the ground pin of the regulator the shorts possible way. If this can not be accomplished separate ground wires for both capacitors should be used (star ground configuration).

6.3 Triggering Reset on OUT2 Ramp Down

To supply large microcomputer systems the current capability of OUT1 may not be sufficient. So it may be helpful to use OUT2 to supply the microcomputer. Now reset supervises the wrong output. This situation can be overcome by using the sense comparator to control OUT2. The output of the comparator is used to discharge the timing capacitor CT. This circuit can be seen on Fig.19.

In this circuit reset will take place if OUT1 drops below 4.7V (pin PR is left open) or if OUT2 drops below 4.5V. Changing the values of R1 and R2 other reset thresholds can be programmed. R3 is just the pull up for the open collector output RES. Depending on the specific application R3 may be connected to OUT2 just as well.

Figure 19: Triggering Reset on OUT2 Ramp Down



6.4 Using the Bandgap Reference of L4938E for auxiliary Circuits

L4938E offers a precision bandgap reference of typically 1.23V at pin PR. If programming the reset threshold to other values than 4.7V is not required this reference can be acessed. The impedance of pin PR is about 100KΩ.

7 CONCLUSIONS

The L4938 and L4938E family is a versatile low consumption voltage regulator family using state of the art technology and circuitry. As far as possible it is designed to meet applicative requirements respecting the posibility of using a low cost capacitors (with high ESR values in the range of several ohms). The major design goal was providing the customer the best possible compromise between precision, low current consumption, dynamic response to distortions and electromagnetic compatibility. Individual parameters of course can be beaten by devices optimised for one feature only sacrifying others (Such as reference circuits that are optimised for precision only, or in the other extreme standard topologies with low precision optimised for dynamic behaviour sacrifying for example current consumption requirements). To provide a good reference (1% at 25 deg. C, 2% throughout the whole temperature range) for precision analogue boards an enhanced bandgap reference circuit is implemented. Samples evaluated show exceptional low drift between 0 deg C and 125 deg. C. Power on reset circuit features proper function downto VOUT1 = V_{be} allowing applications with logic circuits starting to work with low supply voltages. The logic inputs EN and SI are hardened against negative input voltages. The whole circuit is hardened against EMI as far as this is possible at the low quiescent current.